

## IN THE CLAIMS

Amend Claims 1, 6, 7, 15, 17, 18, and 25 as follows:

1. (currently amended) A method of charge-balancing and continuously writing a wafer mask process, comprising:
  - (a) providing a wafer with a plurality of rows;
  - (b) writing a foreground field with charge-balancing features on the wafer, row-by-row, to build critical features for a plurality of magneto resistive (MR) devices on each row to define an MR stripe field;
  - (c) writing additional critical features that define additional boundaries of the MR stripe fields field between each of the charge-balancing features; and
  - (d) writing a background field having non-critical features adjacent to each of the critical features to form a charge-balanced, continuous write wafer mask.
2. (original) The method of claim 1, wherein step (b) comprises writing the charge-balancing features as negative images.
3. (original) The method of claim 1, wherein step (b) comprises writing a pair of charge-balancing features for each MR device, the pair being equal in size and equal in resist charge but spaced apart from each other.
4. (original) The method of claim 3, wherein step (b) comprises placing the charge-balancing features in close proximity to an area where the MR stripe field is written.
5. (original) The method of claim 1, wherein step (b) comprises using a center portion of a glass plate for the MR stripe field.
6. (currently amended) The method of claim 1, wherein step (c) comprises defining the additional critical features as upper and lower edges of the MR stripe fields field.
7. (currently amended) The method of claim 1, wherein step (c) comprises writing the additional critical features in a continuous write mode, pair-by-pair, unfractured, in-line along each row of, and equal distance from the MR devices, such that electromagnetic forces acting on

a writing device that write the MR stripe fields field is equal and, thus, significantly reduces any deflection of the writing device by external motive charging.

8. (original) The method of claim 1, wherein the writing steps comprise using an E-beam.
9. (original) The method of claim 1, wherein step (d) comprises writing the non-critical features in a peripheral area of the background field as positive working images at a relatively larger spot size than the critical images in order to reduce write time.
10. (original) The method of claim 1, wherein step (d) comprises ignoring fracturing and non-continuous writing.
11. (original) The method of claim 1, further comprising overlaying and overlapping the background field with the foreground field.
12. (original) The method of claim 1, further comprising exposing the foreground field before the background field.
13. (original) The method of claim 1, further comprising exposing the foreground field using a same energy and time of exposure as the background field.
14. (original) The method of claim 1, further comprising exposing the resist with the background field so that the charge-balancing features are not exposed into resist by the foreground field.
15. (currently amended) The method of claim 1, wherein each of the background and foreground fields are spaced apart from each other, and further comprising using fields that are angled to span the spaced apart background and foreground fields angle at interfaces where the background and foreground fields intersect to reduce the formation of deviations.
16. (original) The method of claim 15, further comprising adding the angles to the background field, and extending the foreground field above an apex of the background field.
17. (currently amended) A method of charge-balancing and continuously writing a wafer mask process, comprising:

- (a) providing a wafer with a plurality of rows;
- (b) writing a foreground field with charge-balancing features as negative images on the wafer, row-by-row, to build critical features for a plurality of magneto resistive (MR) devices on each row to define ~~[[an]] MR stripe field~~ fields;
- (c) writing additional critical features that define additional boundaries of the MR stripe fields between each of the charge-balancing features, and defining the additional critical features as upper and lower edges of the MR stripe fields; and
- (d) writing a background field having non-critical features adjacent to each of the critical features to form a charge-balanced, continuous write wafer mask.

18. (currently amended) The method of claim 17, wherein step (b) comprises writing a pair of charge-balancing features for each MR device, the pair being equal in size and equal in resist charge but spaced apart from each other, and placing the charge-balancing features in close proximity to an area where the MR stripe ~~field is~~ fields are written.

19. (original) The method of claim 17, wherein step (c) comprises writing the additional critical features in a continuous write mode, pair-by-pair, unfractured, in-line along each row of, and equal distance from the MR devices, such that electromagnetic forces acting on a writing device that write the MR stripe fields is equal and, thus, significantly reduces any deflection of the writing device by external motive charging.

20. (original) The method of claim 17, wherein step (d) comprises writing the non-critical features in a peripheral area of the background field as positive working images at a relatively larger spot size than the critical images in order to reduce write time.

21. (original) The method of claim 17, wherein step (d) comprises ignoring fracturing and non-continuous writing.

22. (original) The method of claim 17, further comprising overlaying and overlapping the background field with the foreground field.

23. (original) The method of claim 17, further comprising exposing the foreground field before the background field, and exposing the foreground field using a same energy and time of exposure as the background field.

24. (original) The method of claim 17, further comprising exposing the resist with the background field so that the charge-balancing features are not exposed into resist by the foreground field.

25. (currently amended) The method of claim 17, wherein each of the background and foreground fields are spaced apart from each other, and further comprising using fields that are angled to span the spaced apart background and foreground fields ~~angles at interfaces where the background and foreground fields intersect~~ to reduce the formation of deviations, and adding the ~~angles~~ angled fields to the background field, and extending the foreground field above an apex of the background field.